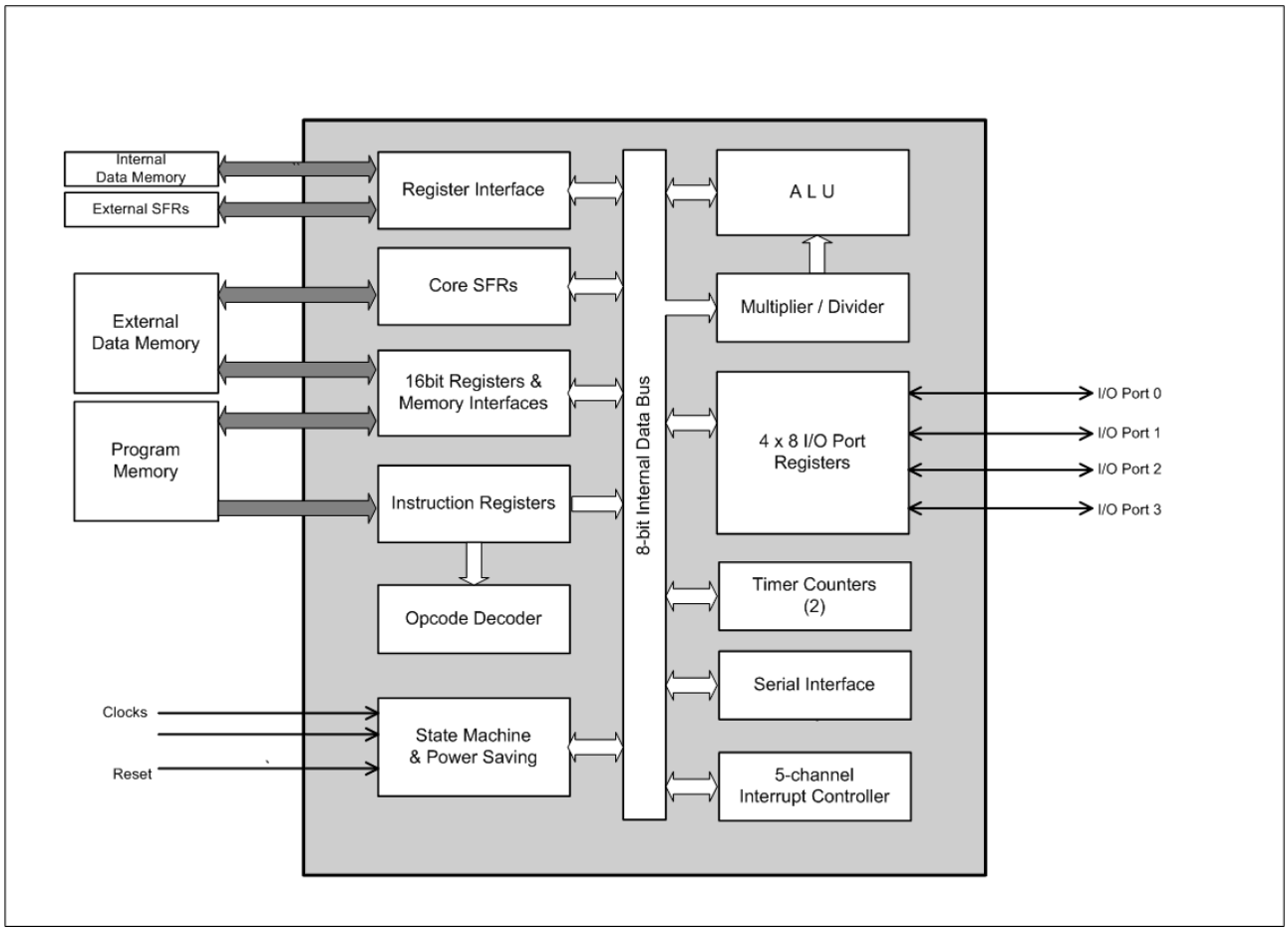
Mentor Graphics M8051
8-bit Microcontroller

Overview

The M8051 is a configurable soft-core implementation of the industry standard 8051 microcontroller that features a clock compatible twelve clocks per machine cycle architecture. This microcode-free design is software compatible (including instruction execution times) with industry standard discrete devices, having all their core features, and the additional features corresponding to the Intel 8051/8031/80C51BH/80C31BH/87C51 parts except that ONCE mode and Program Lock are not supported. The use of standard synchronous design methodology makes this core simple to integrate into both ASIC and FPGA SoC designs.

M8051 Architecture



- Binary and memory cycle compatible with Intel 8051, 8031, 80C51, 80C31, 80C31BH and 87C51
- Classic 12-clock machine cycle implementation
- Up to 64Kbytes program and external data address spaces
- Up to 256 bytes of internal data memory
- Support for memory banking extensions
- Program memory download mode
- 5-input, five level interrupt controller
- 32 GPIO ports
- Two 16-bit counter timers
- Full-duplex serial port
- Flexible interfacing options for external peripherals, including support for external SFRs, five of which may be bit-addressable
- Power saving modes: powerdown and idle
- Fully synthesizable and Scan test ready

Mentor Graphics M8051 8-bit Microcontroller

Configuration Options

The core RTL is highly configurable at compile time allowing users to implement only the features required by their application.

Major configuration options include:

- Combined program and data address space or Harvard architecture
- Code memory size
- External data memory size
- Internal data memory size

Serial Port and Timer/Counters: These are important features of both the original device and the M8051, simplifying the system design required for a range of possible applications. The serial port is full-duplex. It is also receive buffered, allowing the next byte to be received before the previous byte has been read from the receive register.

Data & Program Memory: The M8051 can address internal data memory of up to 256 bytes and internal program RAM or ROM of up to 64K bytes via the functional interconnect signals. The M8051 can also address up to 64K bytes of external data RAM, and 64K bytes of external program ROM via the I/O ports.

Program Memory Download (DLM) Mode: Program memory may be implemented in RAM, and read/write access to this memory is provided so that it may be "downloaded" from the host CPU.

Memory Size Register: The function of this register is to allow a configurable internal memory size for the device. The minimum allowed is 256 bytes, the maximum is 64K bytes.

External Special Function Registers: Up to 106 external special function registers (ESFRs) may be added to the M8051 core. ESFRs are memory mapped into direct memory between addresses 80 hex and FF hex in the same manner as core SFRs and may occupy any address that is not occupied by a core SFR. ESFRs located at C0, C8, D8, E8 or F8 will be bit-addressable.

Power Management

The M8051 offers two power saving states. In the idle state the CPU is stopped while the peripherals continue to run. In the powerdown state all clocks are stopped. These are implemented by dividing the core logic into several synchronous clock domains using optional clock gates. These reduce power consumption by 75% in the idle state and to leakage levels in the powerdown state. The microcontroller can be awoken from the idle state using interrupts.

Programming Support

The core runs all standard 8051 binary code. Syntill8 recommends Keil C51 and IAR Systems compilers for code development.

Deliverables

- VHDL '93 and Verilog 2001 RTL source code
- VHDL and Verilog testbenches
- Demonstration assembly code
- Simulation scripts for Modelsim and Cadence
- Example Synopsys synthesis compile scripts and SDC timing constraint files
- Example Mentor DFT and ATPG scripts
- Example netlist implementation with SDF files
- Detailed product specification and a user guide containing implementation notes

M8051 Product Selector

Design	Clocks per Machine Cycle	External Address Space	Internal Data Memory	Multiplexed External Memory Bus	Wait States Support	Synchronous Memory Support	Interrupt Sources	Non-maskable Interrupt	Interrupt Levels	Data Pointers	I/O ports	Timer Counters	Serial Port	Memory Banking	External SFR Interface	On-chip Debug
M8051	12	0-64K	0-256	✔			5		2	1	32	2	1	✔	✔	
M8052	12	0-64K	0-256	✔			6		2	1	32	3	1	✔	✔	
M8051W	2	0-1M	0-256	✔	✔	✔	05-25	✔	3/5	1/2/4/8	0/32	0/2/3	0/1	✔	✔	
M8051EW	2	0-1M	0-256	✔	✔	✔	05-25	✔	3/5	1/2/4/8	0/32	0/2/3	0/1	✔	✔	✔