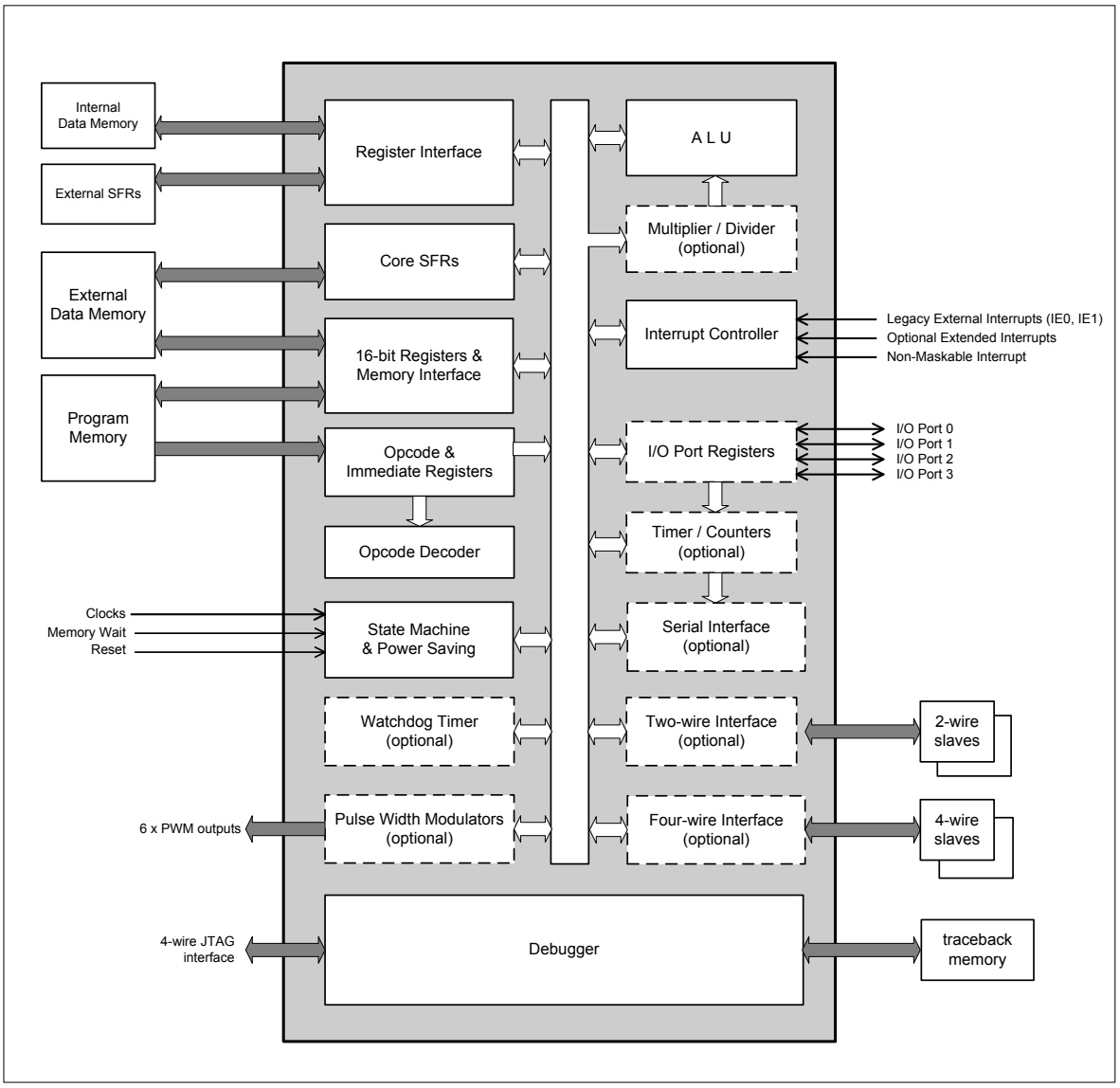
Mentor Graphics M8051EW Fast 8-bit Microcontroller with On-chip Debug

Overview

The M8051EW is a highly configurable soft-core implementation of the industry standard 8051 microcontroller that features a two-clocks-per-machine cycle architecture. Use of standard synchronous design methodology makes this core simple to integrate into both ASIC and FPGA SoC designs.

M8051EW Architecture



- Binary and Memory cycle compatible with the Intel 8051
- Fast 2-clocks per machine cycle implementation
- Richly featured hardware debugger: multiple breakpoints, instruction traceback, single step execution. Full access to all address spaces
- 1Mbyte program and data address spaces
- Memory interfaces all support wait states and may be configured for synchronous or asynchronous devices
- Optional de-multiplexed program and data interfaces
- Optional single machine cycle memory accesses
- Optional conditional branch acceleration
- Up to eight 16-bit data pointers
- 25-input, five level interrupt controller
- Optional full implementation of legacy peripherals: 32 GPIO ports, 3 16-bit counters and full-duplex serial port
- Watchdog timer
- 2-wire and 4-wire master interfaces
- Pulse width modulator array
- Flexible interfacing options for external peripherals
- Power saving modes: powerdown, stasis, idle and run

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Configurable

The core RTL is highly configurable at compile time allowing users to implement only the features required by their application.

Major configuration options include:

- Combined program and data address space or Harvard architecture
- Optional 20-bit (1Mbyte) extended memory addressing scheme with additional stack
- 1, 2, 4 or 8 16-bit data pointers
- Each memory component may use a synchronous or asynchronous interface
- Hardware multiplier/divider is optional
- Up to 25 interrupt sources with up to 5 priority levels
- All peripherals are optional and may be excluded if not required
- Debug traceback depth and number of hardware triggers are selectable

Configurable Peripherals

The core includes the following peripherals as standard:

- Three timer/counters
- Legacy UART
- Watchdog timer
- Two-wire master interface
- Four-wire master interface
- Pulse width modulator array, with ramping option

All non-legacy peripherals include a configurable clock prescaler, and configurable base addresses and interrupt channels.

Power Management

The M8051EW offers three power saving states. These are implemented by dividing the core logic into several synchronous clock domains using optional clock gates. These reduce power consumption by 75% in the idle state and to leakage levels in the stasis and powerdown states. The microcontroller can be awoken from idle and stasis states using interrupts.

Programming Support

The core runs all standard 8051 binary code. Syntill8 recommends Keil C51 and IAR Systems compilers for code development. These compilers can optimise code by making use of the M8051EW data pointer and interrupt extensions.

Debug Support

The M8051EW includes comprehensive on-chip instrumentation accessed by external debug environments via a four-wire JTAG port. Debug features include start/stop/step/ hardware and software breakpoints, execution traceback, and full read/write access to all memory and SFR locations. The M8051EW debug interface is designed to be compatible with FS2 System Navigator debug system.

Deliverables

- VHDL '93 and Verilog 2001 RTL source code
- RTL configuration script
- VHDL and Verilog testbenches
- Demonstration assembly code
- Simulation scripts for Modelsim and Cadence
- Synopsys synthesis compile scripts and SDC timing constraint files
- Example Mentor DFT and ATPG scripts
- Example netlist implementation with SDF files
- Detailed product specification and a user guide containing implementation notes

M8051 Product Selector

Design	Clocks per Machine Cycle	External Address Space	Internal Data Memory	Multiplexed External Memory Bus	Wait States Support	Synchronous Memory Support	Interrupt Sources	Non-maskable Interrupt	Interrupt Levels	Data Pointers	I/O ports	Timer Counters	Serial Port	Memory Banking	External SFR Interface	On-chip Debug
M8051	12	0-64K	0-256	✔			5		2	1	32	2	1	✔	✔	
M8052	12	0-64K	0-256	✔			6		2	1	32	3	1	✔	✔	
M8051W	2	0-1M	0-256	✔	✔	✔	05-25	✔	3/5	1/2/4/8	0/32	0/2/3	0/1	✔	✔	
M8051EW	2	0-1M	0-256	✔	✔	✔	05-25	✔	3/5	1/2/4/8	0/32	0/2/3	0/1	✔	✔	✔