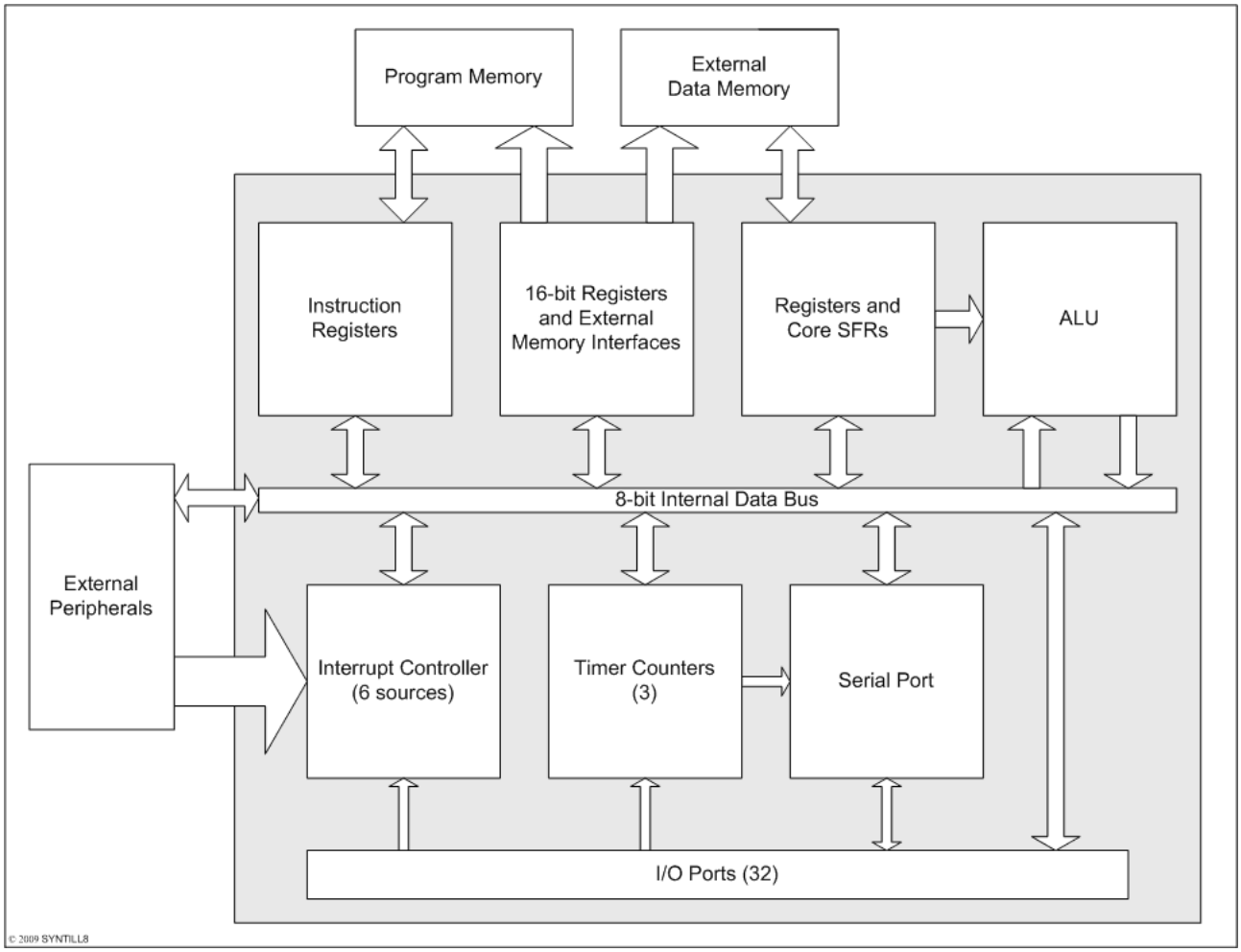
Mentor Graphics M8052
8-bit Microcontroller

- Binary and clock cycle compatible with Intel 8051 designs
- Classic 12-clock machine cycle implementation
- Separate data and code address spaces (Harvard architecture)
- 64Kbyte program and data address spaces
- 256 byte internal data memory address space
- Support for memory banking extensions
- Optional demultiplexed program and data interfaces.
- 6-input, two level interrupt controller
- 32 GPIO ports
- 3 16-bit counter timers
- Full-duplex serial port
- Flexible interfacing options for external peripherals
- Power saving modes: powerdown, idle and run

M8052 Architecture



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Overview

The M8052 is a highly configurable soft-core implementation of the industry standard 8051 microcontroller that features a clock-compatible twelve-clocks-per-machine cycle architecture. Use of standard synchronous design methodology makes this core simple to integrate into both ASIC and FPGA SoC designs.

Configurable

The core RTL is configurable at compile time. Major configuration options include:

- Combined program and data address space or Harvard architecture
- code memory size
- external data memory size
- internal data memory size

Power Management

The M8052 offers two power saving states. These are implemented by dividing the core logic into two synchronous clock domains using optional clock gates. These reduce power consumption by 75% in the idle state and to leakage levels in the powerdown state.

Programming Support

The core runs all standard 8051 binary code. Syntill8 recommends Keil C51 compiler for code development.

Deliverables

- VHDL '93 and Verilog 1995 RTL source code
- RTL configuration script
- VHDL and Verilog Testbenches
- Demonstration assembly code
- Simulation scripts for Modelsim and Cadence
- Synopsys synthesis compile scripts and UCF timing constraint files.
- Mentor and Synopsys DFT and ATPG scripts
- Example netlist implementation with SDF files
- Detailed product specification and a user guide containing implementation notes.

M8051 Product Selector

Design	Clocks per Machine Cycle	External Address Space	Internal Data memory	Multiplexed External Memory Bus	Wait States Support	Synchronous Memory	interrupt Sources	Non-maskable Interrupt	Interrupt Levels	Data Pointers	I/O ports	Timer Counters	Serial Port	Memory Banking	External SFR Interface	On-chip Debug
M8051	12	0-64K	0-256	I			5		2	1	32	2	1	I	I	
M8052	12	0-64K	0-256	I			6		2	1	32	3	1	I	I	
M8051W	2	0-1M	0-256	I	I	I	05/24	I	3/5	1/2/4/8	0/32	0/2/3	0/1	I	I	
M8051EW	2	0-1M	0-256	I	I	I	05/24	I	3/5	1/2/4/8	0/32	0/2/3	0/1	I	I	I