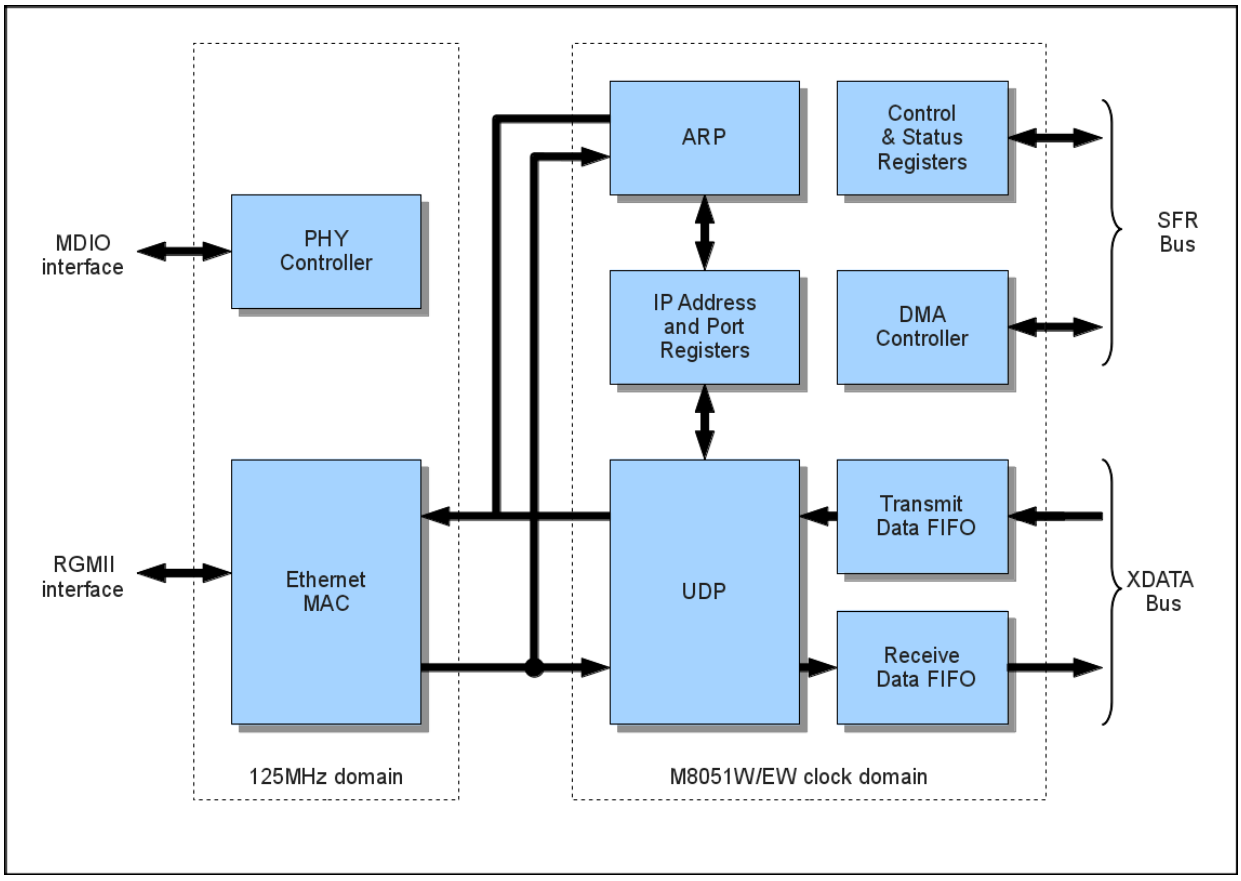
UDPMAC
UDP Network Interface with Ethernet MAC for the M8051W and M8051EW

Overview

The UDPMAC adds IP networking capability to the M8051W and M8051EW IP designs. Use of standard synchronous design methodology makes this core simple to integrate into both ASIC SoC and FPGA designs.

UDPMAC Network Interface Structure



- Simple IP datagram interface providing transport–level exchange of data over IP networks
- Compatible with the RFC768 UDP specification
- Includes a simple ARP protocol handler, suitable for point-to-point connections to switches
- An RFC894 compatible Ethernet MAC
- Integral MDIO controller interfaces to external PHY devices using a 1 gigabit RGMII interface
- Programmable MAC, IP and port addresses
- DMA controller automates data transfers between network and host data memory, interrupt and SFR buses with no additional glue logic required
- Integral transmit and receive data FIFOs minimise the processor overhead required to service the link
- Supports DMA, interrupt-driven and polled data transfers
- Asynchronous data FIFOs enable host clock to operate asynchronously to the PHY clock
- Optional clock prescaler minimises power consumption while active
- Rests in power saving mode when the interface is not enabled
- Wake up on MAC address, or IP address match, can be used to cold start a M8051W and M8051EW microcontroller, in addition to interrupt driven wake ups
- Binds tightly to M8051W and M8051EW external data buses

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Supported Protocols

The UDPMAC implements a UDP transport layer, and IP layer functions, compatible with the RFC768 and RFC791 protocols.

The UDPMAC also includes Ethernet Media Access Controller (MAC) functionality that is compatible with the RFC894 protocol. The MAC interfaces to an external PHY using the 4-wire RGMII gigabit interface. The PHY can be controlled using the UDPMAC via a four-wire MDIO interface.

The integral ARP protocol handler enables the UDPMAC to autonomously identify itself on networks and respond to ARP MAC address requests. The ARP logic includes a single-depth cache suitable for identifying the remote device on a point-to-point connection.

Interfacing

The UDPMAC is designed to bind closely to the M8051W and M8051EW with minimal additional glue logic. Data is exchanged with the host M8051W and M8051EW XDATA memory using an integral DMA controller. The DMA logic generates an interrupt for each segment transfer. Pointer registers identify the current position of the transmit and receive buffers.

Data, control and status information are exchanged with a host microcontroller using the memory-mapped 8-bit SFR bus. This interface allows the host to program address registers, DMA configuration, and PHY control words.

A single interrupt signal is used to indicate that a matching address has been received, that data buffers require service or that an exception has been detected.

Structure

The UDPMAC is comprised of two independent clock domains: The 125MHz Ethernet MAC domain and the host peripheral domain. Generally the host clock frequency is either the same or higher than the Ethernet clock's. The host clock domain can be stopped between packets; however the Ethernet domain runs continually whilst the device is attached to the network.

Data segments are exchanged either by direct access to the host's XDATA memory using the UDPMAC's DMA controller, or alternatively using transmit and receive FIFOs for interrupt-driven transfer.

MAC, IP and port address filters ensure that unwanted packet data is not stored in host memory.

Configuration Options

The core RTL is highly configurable at compile time allowing users to implement only the features required by their application. Major configuration options include:

- DMA or FIFO based data path
- Configurable data FIFO depths up to 1500 bytes
- Single clock design, or independent MAC and microcontroller clock domains
- User defined SFR base address
- User defined interrupt channel
- Optional microcontroller wake-up signal on MAC address match, MAC broadcast, IP address match, or IP and port address match

Power Management

The UDPMAC is compatible with the standard M8051W and M8051EW core three power saving states. In the M8051W and M8051EW idle state the UDPMAC continues to function, transferring data in or out of data FIFOs and generating an interrupt when a transfer is complete or a FIFO requires attention. In DMA implementations, the host XDATA memory is additionally clocked during idle modes to facilitate the transfer of packet data.

A clock prescaler enables designs to select the minimum clock frequency for correct operation of the UDPMAC logic.

The UDPMAC can be configured to generate a host wake-up signal whenever the device select is detected. This enables the host logic to be left in a deep power saving state between Ethernet messages.

Deliverables

- VHDL '93 and Verilog 2001 RTL source code
- VHDL and Verilog functional demonstration testbench
- Demonstration assembler code
- Simulation scripts for Modelsim and Cadence
- Synopsys synthesis compile scripts and SDC timing constraint files
- Example Mentor DFT and ATPG scripts
- Example netlist implementation with SDF files
- Detailed product specification and a user guide containing implementation notes